

Keysight Technologies

Scanning Microwave Microscopy for
Semiconductor Failure Analysis

Application Note

Introduction

Failure analysis is a vital process in the development of a new product and/or improvement of existing products in the semiconductor industry. Successful failure analysis can identify the root cause of a failed device and guide through corrective actions. Semiconductor failure analysis often involves a number of different techniques, such as curve tracing, scanning electron microscopy, transmission electron microscopy, microthermography, focused ion beam analysis, etc. As a relatively new tool, atomic force microscopy (AFM) based techniques, such as scanning capacitance microscopy, conductive AFM, and scanning spreading resistance microscopy, have been applied to analysis of various failed devices [1]. In this article, the recently developed scanning microwave microscopy (SMM) [2-5] demonstrates, for the first time, its capability of doing semiconductor failure analysis.

The scanning microwave microscope (SMM) combines the capability of high spatial resolution of an atomic force microscope (AFM) with the feature of high sensitivity of electric measurements of a vector network analyzer (VNA). In an SMM [2], an incident microwave signal generated from the network analyzer passes through a matched resonant circuit in the AFM, and reaches the end of a conductive probe which is in contact with a surface. The reflected microwave from the contact point is sensed by the probe and returned to the network analyzer. By measuring the complex reflection coefficient, or S11 parameter, the capacitance/impedance at the contact point is obtained from the network analyzer. In practice, the mapped signals are the logarithm of the reflection coefficient amplitude, labeled as VNA amplitude, and VNA phase. From the VNA amplitude and phase values, the contact capacitance/impedance can be derived after proper calibration. In this failure analysis work, only qualitative measurements were used.

When a metal probe is in contact with a silicon surface, it forms a metal-oxide-semiconductor capacitor which is well studied in semiconductor physics [6]. The total capacitance, in the simplified one dimensional model, comes from contributions of two capacitors connected in serial: the surface oxide dielectric layer with a fixed capacitance and the underneath depletion layer in the silicon substrate with a variable capacitance. The capacitance variation of the depletion layer in response to an applied ac bias is determined by the depletion depth, which is in turn largely affected by the dopant concentration in the substrate. Therefore, by measuring the capacitance change induced by the applied AC bias, or dC/dV , the dopant concentration at each contact point can be mapped. Any failure due to abnormal dopant concentration can be then identified from the dC/dV image, simultaneously with the capacitance image measured from the VNA amplitude signal.

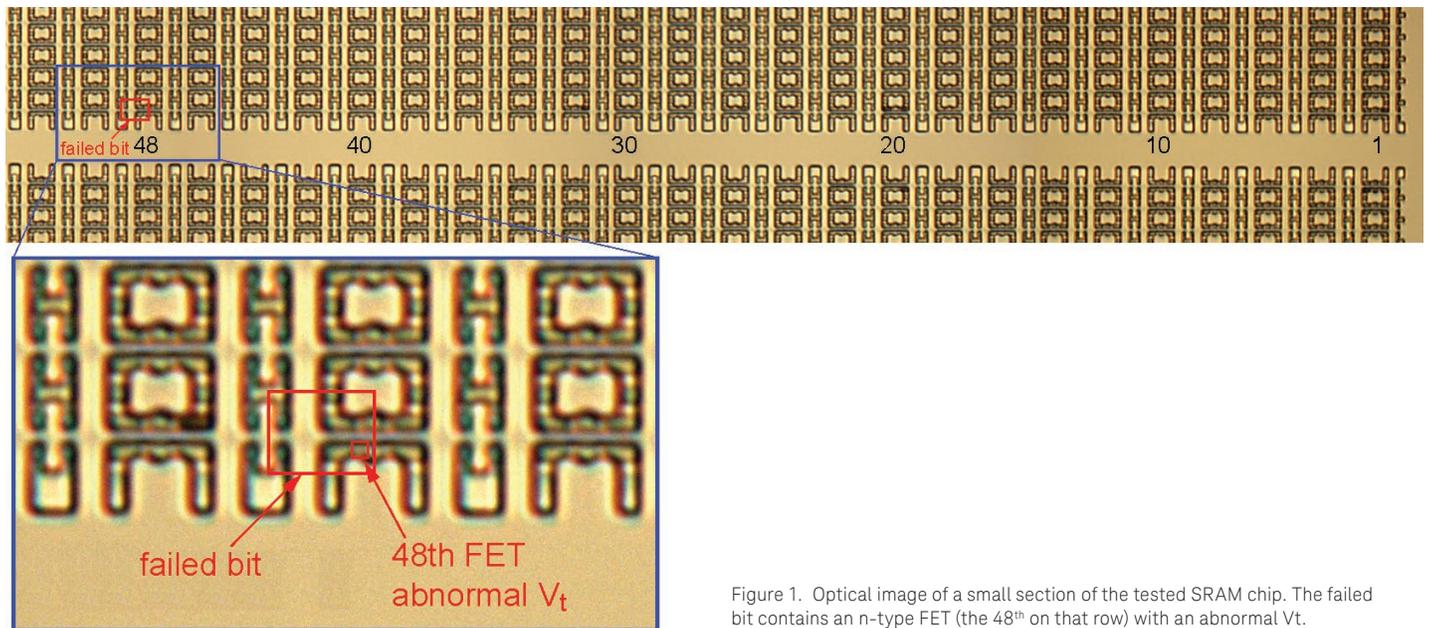


Figure 1. Optical image of a small section of the tested SRAM chip. The failed bit contains an n-type FET (the 48th on that row) with an abnormal V_t .

Experiment

The sample being tested was a depackaged 250 nm static random access memory (SRAM) chip. A standard SRAM unit bit cell contains six field effect transistors (FETs), two p-type FETs in an n-doped well and four n-type FETs in a neighbor p well. Among thousands of bit cells on the chip, one failed. Inside the failed bit, one n-type FET was measured having an abnormal threshold voltage V_t . It was the 48th n FET on that row, as shown in Figure 1. Scanning microwave microscopy was tried, attempting to find any unusual properties of the transistor different from other normal transistors.

Both pure Pt metal probes and conductively coated silicon probes were used. The Pt metal probe was 300 to 400 μm long, made of solid platinum mounted on an aluminum substrate. Its spring constant was estimated from 0.3 to 0.8 nN/nm, and its tip radius of curvature was approximately 10 to 20 nm. The silicon probe was 125 μm long, coated with 20 nm Ti and 10 nm Pt. Its nominal spring constant was 5 nN/nm with tip radius of about 40 nm. Both types of probes showed consistent SMM results on the SRAM chip.

Scanning was carried out in ambient in contact mode. Selected microwave operation frequencies were between 2 to 5 GHz. The low frequency modulation was around 80 kHz. Scan rate was typically from 0.5 to 1 line/sec.

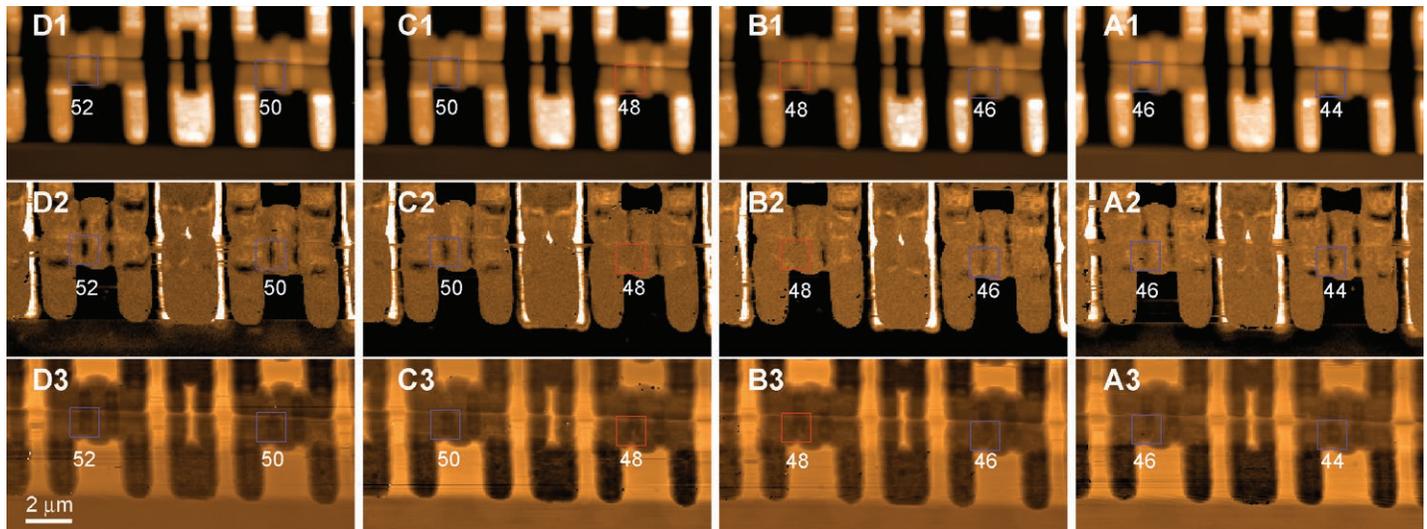


Figure 2. Four sets (A, B, C, and D) of scanning microwave microscopy images on the failed SRAM chip. Each set contains topography (top), dC/dV (middle), and VNA amplitude (bottom) images acquired simultaneously. The red squares outlined the failed 48th n-type FET, and the blue squares are normal n FETs on the same row.

Results

To accurately identify any possible problem with sufficient details, every two pairs of FETs on the same row as the failed FET were scanned, from the 43rd/44th pair through the 51st/52nd pair, as shown in Figure 2. Total of four sets of images (A, B, C, and D) were acquired under the same conditions. Each set contained topography (top), dC/dV (middle), and VNA amplitude (bottom) images obtained simultaneously. For illustration purposes the even number n-type FETs on the same row as the failed FET were outlined with squares in all images.

The topography images of the 48th n FET, outlined by the red squares in Figures 2 B1 and C1, didn't appear to have any structural difference compared to the normal n FETs (blue squares as well as the unmarked ones in all of the topography images). They were also very similar to those seen on other SRAM samples [2, 4]. In the dC/dV images, however, the difference was quite noticeable. Every normal n FET (blue square) consistently showed a dark area near the center. The dark (low) value in the dC/dV image represented p-type dopant of the well in the channel. The 48th n FET, on the other hand, was completely flat without any contrast, as shown in the red squares of both Figures 2 B2 and C2. The missing p-dopant signal in the 48th n FET clearly indicated a change of dopant structure of the channel area of the transistor. The VNA amplitude images of the 48th n FET, when examined carefully from Figures 2 B3 and C3, also showed a different structure from the other normal n FETs. It indicated a different capacitance/impedance value.

Conclusions

Scanning microwave microscopy has demonstrated its capability of doing semiconductor failure analysis. Images of dopant concentration measured from the dC/dV signal on a defect SRAM chip clearly identified an unusual dopant structure of the failed n FET, different from other normal n FETs. Capacitance images measured from the VNA amplitude also showed a slight different contrast of the transistor. This experiment has shown that the scanning microwave microscope can be a convenient direct-imaging tool to probe a variety of electric failures in semiconductor devices not visible from surface topography structure on scales of micrometers to nanometers.

References

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